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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,016	06/30/2003	Kazutaka Shibata	AI 288	1927

7590 06/15/2006

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EXAMINER

IM, JUNGHWA M

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/608,016

Applicant(s)

SHIBATA, KAZUTAKA

Examiner

Junghwa M. Im

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 3,4 and 8-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 3,4 and 8-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>5/2006, 1/2006</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites a limitation of “the resin film is a first resin, comprising a second resin film ... on the other side of the semiconductor substrate.” Note that the resin film on the back cannot meet the subsequent limitation for example, forming an interface of the passivation/resin layer. Furthermore, the figures 4 and 5 of the instant invention that is recited in the independent claim 8 do not show this aspect.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Wakamiya et al. (US Pat. Pub. 2002/0041013), hereinafter Wakamiya.

Regarding claim 8, Fig. 1 of Wakamiya shows semiconductor device, comprising:

a semiconductor chip (1);

an electrode pad (2) formed on the semiconductor chip;

a resin film (5) formed to cover a surface of the semiconductor chip; and

a post (4, 10) bonded to the electrode pad and provided to penetrate through the resin film, a portion (10) of which in close proximity to a junction portion with the electrode pad is made of gold (paragraph [0023]); and

a passivation layer (3) on the surface of the semiconductor chip, between the semiconductor chip and the resin film and covered by the resin film so as to have a passivation film/resin film interface therein, the gold portion of the post including a portion facing the passivation film/resin film.

Regarding claim 9, Fig. 1 of Wakamiya shows that the post includes a portion made of a metal material other than gold (paragraph [0023]).

Regarding claim 10, Fig. 1 of Wakamiya shows that the post includes a junction portion provided on a side of the electrode pad and made of gold, a tip end portion provided on a side of a tip end and made of gold and an intermediate portion provided between the junction and the tip end portion and made of a metal other than gold (paragraph [0021]).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (US Pat. Pub. 2005/0167808), hereinafter Sasaki in view of Tanaka et al. (US 6147374), hereinafter Tanaka and Eguchi et al. (US 6627997), hereinafter Eguchi

Regarding claim 3, Fig. 12 of Sasaki shows a semiconductor device, comprising:

a semiconductor substrate (1);

at least one of a protruding electrode (3) and wiring (1B) formed on one surface of the semiconductor substrate; and

a first resin film (1D; polyimide protection film) formed on the one surface of the semiconductor substrate; and

a second resin film (2; thermosetting resin).

Fig. 12 of Sasaki shows most aspects of the instant invention except that “the first resin film has elasticity lower enough to reduce stress induced by a difference in thermal expansion coefficient between the semiconductor substrate and the first resin film” and “a second resin film having one of higher and higher strength than the first resin film is formed on the other surface of the semiconductor device.” Tanaka teaches a surface protective film made of polyimide having an elastic modulus 2600MPa - 6 GPa (col. 3, line 65 - col. 4, line 7).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Tanaka into the device of Sasaki in order to have the

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first resin film having elasticity lower enough to reduce stress induced by a difference in thermal expansion coefficient between the semiconductor substrate and the first resin film to improve the reliability of the device.

The combined teachings of Sasaki and Tanaka fail to show that “a second resin film having one of higher and higher strength than the first resin film is formed on the other surface of the semiconductor device.” Eguchi teaches a thermosetting resin having an elastic modulus 500MPa - 25 GPa (col. 6, lines 12-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Eguchi into the device of Sasaki and Tanaka in order to have a second resin film having one of higher and higher strength than the first resin film is formed on the other surface of the semiconductor device to improve the endurance.

Regarding claim 4, Eguchi discloses that an elastic modulus of the second resin film is 15 GPa or higher.

Regarding claim 6, the combined teachings of Sasaki, Tanaka and Eguchi shows substantially the entire claimed structure including that the semiconductor substrate is placed at a center of the semiconductor except “the semiconductor substrate has a thickness of 200  $\mu\text{m}$  or less.” However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have the semiconductor substrate with a thickness of 200  $\mu\text{m}$  or less to reduce a package size, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller*, 105 USPQ 233.

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Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakamiya in view of Shieh et al. (US Pat. Pub. 2002/0056741), hereinafter Shieh.

Regarding claim 11, Fig. 1 of Wakamiya shows most aspects of the instant invention including the passivation layer has a thickness greater than a thickness of the electrode pad, however, fails to show that “the gold portion of the post projects below a surface of passivation layer at the passivation film/resin film interface into direct contact with the electrode pad.” Fig. 9a of Shieh shows a lower portion of a gold post (61) projects below a surface of passivation layer (12) at the passivation film/resin film interface into direct contact with the electrode pad (11).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teachings of Shieh into the device of Wakamiya in order to have a lower portion of a gold post projecting below a surface of passivation layer at the passivation film/resin film interface into direct contact with the electrode pad for easier soldering to the pad.

Regarding claim 12, Fig. 1 of Wakamiya shows most aspect of the instant invention including the passivation layer has a thickness greater than a thickness of the electrode pad, however, fails to show that “the gold portion of the post projects below a surface of passivation layer at the passivation film/resin film interface into confrontation with the electrode pad.” Fig. 9a of Shieh shows a lower portion of a gold post (61) projects below a surface of passivation layer (12) at the passivation film/resin film interface into confrontation with the electrode pad (11).

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It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teachings of Shieh into the device of Wakamiya in order to have a lower portion of a gold post projecting below a surface of passivation layer at the passivation film/resin film interface into confrontation with the electrode pad for easier soldering to the pad.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wakamiya as applied to claim 8 above, and further in view of Sasaki in view of Tanaka et al. (US 6147374), hereinafter Tanaka and Eguchi et al. (US 6627997), hereinafter Eguchi.

Regarding claim 13, insofar as understood, Wakamiya shows most aspect of the instant invention except "a second resin film having one of higher and higher strength than the first resin film is formed on the other surface of the semiconductor device." Sasaki discloses the resin films on the front and the back of the semiconductor device. And Tanaka shows the resin film on the front teaches a surface protective film made of polyimide having an elastic modulus 2600MPa - 6 GPa (col. 3, line 65 - col. 4, line 7). Eguchi teaches a thermosetting resin having an elastic modulus 500MPa - 25 GPa (col. 6, lines 12-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Sasaki, Tanaka and Eguchi into the device of Wakayama in order to have a second resin film having one of higher and higher strength than the first resin film is formed on the other surface of the semiconductor device to improve the endurance.



***Response to Arguments***

Applicants' arguments with respect to pending claims 3-4 and 6 have been considered but are moot in view of the new ground(s) of rejection.

And Applicants' arguments on claims 8-13 have been fully considered but they are not persuasive. Applicants argue that "... the gold stress-absorbing layer 10 of *Wakamiya et al.*, which is provided at the middle of a post 4, does not face the interface between a coating layer 7 and the protective dielectric layer 3 or the interface between the protective dielectric layer sealing resin 5, as would be required if the reference were to meet the requirements of the claim. Thus, the stress-absorbing layer 10 fails to meet the gold portion of the post in the present invention of claim 8 that requires the gold portion face the passivation film/resin film interface." Note that the instant invention does not recite these aspects. Rather, the instant invention recites that "a post bonded to the electrode pad and provided to penetrate through the resin film, a portion of which in close proximity to a junction portion with the electrode pad is made of gold," indicating that a portion of the post near the connection to the pad is made of gold. *Wakamiya* shows this as stated in the office action above. And the instant invention further recites that "a passivation layer on the surface of the semiconductor chip, between the semiconductor chip and the resin film and covered by the resin film so as to have a passivation film/resin film interface therein, the gold portion of the post including a portion facing the passivation film/resin film," indicating that the resin layer is formed on the passivation layer, therefore, forming an interface of a passivation film/resin film. And this limitation further indicates that a portion of the gold portion of the post is facing the interface of the passivation

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film/resin film. Wakamiya shows that the bottom of the gold post is facing the interface of passivation film/resin film.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

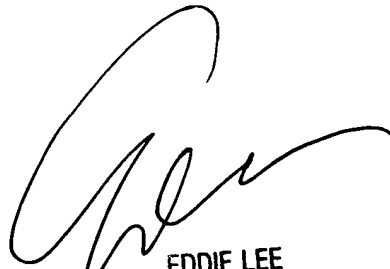
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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